

**MARK S. HARRIS**  
4105 Dauphine Dr. • Austin, TX 78727  
512-719-4489  
MarkSHarris@austin.rr.com

---

### SUMMARY

Hands-on Electrical/Hardware Engineer with extensive experience in System Architecture Design, Circuit Design, Logic Design, Microprocessor Interfacing. Ability to do both hardware and software. Strong ability to work individually or as part of a team from project conception through verification, including interfacing with Electrical, Mechanical, Test and Manufacturing teams. Excellent ability to visualize solutions and solve technical issues.

#### Product Design Proficiency:

System Architecture, Product Definition and Specification. Digital Circuit Design. PLD & FPGA design, Power distribution.. Mentor and Cadence Schematic Capture and Layout tools. Have designed circuit boards for both high volume production and high performance testcard and product environments. Most designs have involved controlled impedance, differential pairs, controlled topology routing and other constraints needed for high speed digital systems.

#### Application Software Proficiency:

Abel, Palasm and VHDL hardware languages. Python, C, Pascal, FORTRAN and various assembly languages. Microsoft Office and Visio, Adobe FrameMaker. Experience with various operating systems including Windows, Mac and Unix.

### PROFESSIONAL ACCOMPLISHMENTS

#### **DELL, Austin, TX 2007**

##### **Senior Electrical Engineer**

- Implemented power system for new server series.

#### **CELESTICA, Austin, TX 2005 –2006**

##### **Senior Electrical Engineer**

- Assigned directly to IBM Corporation as a member of the server design team.
- Designed 3+ Gigahertz Power6 processor board for mid-level eClipz series servers.
- Debugged various in-house developed engineering tools.

#### **MOTOROLA SEMICONDUCTOR DIVISION/FREESCALE SEMICONDUCTOR, Austin, TX 1982-2004**

##### **Senior Electrical Engineer, 1991-2004**

- Produced numerous processor cards for a variety of PowerPC processors, allowing these chips to be quickly tested, debugged and brought to market in less time and money than using production chip testers.
- Created a series of Gigabit Ethernet Boards to test processor RMII, MII, GMII, TBI, RGMII, RTBI interfaces both with and without commercial PHY chips.
- Designed complex four-processor 128-bit data bus processor card.
- Produced processor card with high-speed L2 cache memory for Apple and Apple-clone computers which brought in \$140 million profit.
- Designed highly configurable PCI backplane board used for testing new PCI controller chips.
- Devised bridge module allowing the processor cards from the older test system to be used on the newer system saving money and development time. This bridge also brought new verification techniques to the older system, speeding up and improving chip verification.

- Developed temperature control system for processor test using thermo-electric coolers coupled with vortex tubes. Vortex tubes turn compressed air into a cooling (or heating) air stream with no moving parts. This allowed precise control of a processor's temperature, cost less than \$3000 and took up less space than the stand-alone freon type lab temperature control units, which cost over \$15K.
- Implemented flexible, distributed power distribution including power monitoring for several testcard systems allowing for unknown changes in future processors yet protecting the systems from user errors and electronic failures.
- Designed flexible high-current plug-in power module boards to supply core power for processors under test, assuring improved response times and protecting from part obsolescence.
- Created a test coupon board with various line topologies, line characteristics and termination techniques to test new processor IO drivers and to verify PCB simulation models.

### **MOTOROLA COMPUTER GROUP, Austin, TX**

#### **Electrical Engineer, 1982-1991**

- Extended the VSBbus (secondary bus for VMEbus) from the original four inches to four feet allowing it to be used as a high-speed secondary bus for a family of remote IO and disk boards. Created a prototype proving the concepts and determining the appropriate cable characteristics needed. Designed the first IO board for this system.
- Created In-house test and development VME board for the 68030 processor and the VME and VSB gate array chips. This card became the core of all future Motorola 68030 and 68040 VMEbus products.
- Chief architect of the Motorola VME Master/Slave gate array chip. This became the VME interface used on all Motorola VMEbus processor boards for several years.
- Pioneered first Motorola VMEbus memory board using SIP memory modules, the first using a mezzanine board and the first using ZIP memory packaging.
- Designed the industry's first 32-bit VMEbus dynamic memory board, increasing sales of the companion 32-bit processor board.
- Conducted the initial study of microcomputer-based workstations for electronic design for the Motorola Computer Group. Narrowed the choice down to two companies, Valid (now Cadence) and Mentor. Both are still in business while most of the others are long since gone.

### **EDUCATION & TRAINING**

**B.S. Electrical Engineering.** University of Texas, Austin, TX

#### **As an Engineering Co-op Student at VOUGHT CORPORATION, Grand Prairie, TX:**

- Added graphics capability to major electrical network simulation program used for design of AIRTRANS transportation system at DFW airport.

#### **As a part-time University of Texas employee:**

- Carried out various graphics programming and software conversion projects for the Associate Dean of Engineering.
- Selected and set up the first microcomputer system for the Chemical Engineering laboratory.

Mentor Comprehensive VHDL

High-Speed Digital Design by Dr. Howard Johnson

Advanced High-Speed Signal Propagation by Dr. Howard Johnson

### **PUBLICATIONS**

"A Chip for All Boards". ESD, February 1988

"Die Dynamische Busanpassung Wird Unterstützt". VMEbus, February 1988

"VMEchip Unterstützt die Dynamische Busanpassung". Elektronik, March 1988